CLAIMS

What is claimed is:

1. A straddled gate device formed on a semiconductor-on-insulator (SOI) substrate having active regions defined by isolation regions and an insulator layer, the device comprising:

a first gate defining a first channel region interposed between a source and a drain formed within the active region of the SOI substrate;

a second gate straddling the first gate defining second channel regions interposed between the first channel region and the source and the drain; and

a contact connecting the first gate with the second gate wherein when the device is in the off state (I_{off}) the first channel region and second channel regions define a long channel and when the device is in the on state (I_{on}) the first channel region defines a short channel.

2. The straddled gate device according to claim 1, wherein the first gate defines a work function and the second gate defines a second work function.

3. The straddled gate device according to claim 2, wherein the second work function of the second gate is 0.3 – 0.5 eV less than the work function of the first gate.

4. The straddled gate device according to claim 1, wherein the source and the drain include main source and drain regions and source and drain extension regions.

5. The straddled gate device according to claim 1, includes a silicide layer formed on the main source and drain regions.

6. The straddled gate device according to claim 5, wherein the silicide layer which is formed on the main source and drain regions has a thickness in a range between 100 Å and 400 Å.

7. The straddled gate device according to claim 1, including a second silicide layer formed on electrodes of the second gate.

8. The straddled gate device according to claim 7, wherein the thickness of the second silicide layer formed on the electrodes of the second gate has a range between 100 Å and 400 Å.

9. The straddled gate device according to claim 1, wherein the silicide layer formed on the main source and drain regions and the second silicide layer formed on the electrode of the gate are of silicide of different species.

10. The straddled gate device according to claim 1, wherein the semiconductor-on-insulator substrate is a germanium-on-insulator (GOI) substrate.

11. The straddled gate device according to claim 10, wherein the silicide layer which is formed on the main source and drain regions and the source and drain extension regions has a thickness in a range between 100 Å and 400 Å.

12. The straddled gate device according to claim 10, including a second silicide layer formed on electrodes of the second gate.

13. The straddled gate device according to claim 12, wherein the thickness of the second silicide layer formed on the electrode of the gate has a range between 100 Å and 400 Å.

14. The straddled gate device according to claim 13, wherein the silicide layer formed on the main source and drain regions and the second silicide layer formed on the electrodes of the second gate are of silicide of different species.

15. A method of fabricating a straddled gate device formed on a semiconductor-on-insulator (SOI) substrate having active regions defined by isolation regions and an insulator layer, the method comprising the steps of:

forming a first gate defining a first channel region interposed between a source and a drain formed within one of the active regions of the SOI substrate;

forming a second gate straddling the first gate defining second channel regions interposed between the first channel region and the source and the drain; and

forming a contact connecting the first gate with the second gate wherein when the device is in the off state (I_{off}) the first channel region and second channel regions define a long channel and when the device is in the on state (I_{on}) the first channel region defines a short channel.

16. The method according to claim 15, wherein the source and the drain include main source and drain regions and source and drain extension regions.

17. The method according to claim 15, including the additional step of forming a silicide layer on the main source and drain regions.

18. The method according to claim 17, including the additional step of forming a second silicide layer on electrodes of the second gate.

19. The method according to claim 18, wherein the step of forming the second silicide layer on the electrodes of the second gate the second silicide layer is of a different species.

20. The straddled gate device according to claim 15, wherein a work function of the second gate is 0.3 – 0.5 eV less than a work function of the first gate.

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